REMARKS

Claims 13 and 15 - 18

Claim 13 has been rejected under 35 U.S.C. §102(b) as anticipated by U.S. patent no. 6,011,725 ("Eitan"). The Office Action correctly points out that a portion 23 of a charge storage dielectric 18 is disclosed in Eitan to be programmed "to one of two threshold levels" (Office Action, para. 4). But claim 13 as originally presented recites that charge is transferred into a defined region of the charge storing dielectric to adjust a threshold of the cell into more than two threshold levels. This is submitted to have rendered the claim novel. But in order to make sure that this feature is clearly recited, claim 13 has been amended to state that charge is controlled in each of at least two dielectric regions to program each region into one of more than two threshold levels according to the data being stored. Eitan does not suggest that either of its charge storage regions 21 or 23 can be programmed to more than two levels of charge. In addition to this change, other features have been added to claim 13 that are also included in the remaining claims discussed below, in order to make them consistent. Reconsideration of amended claim 13 is respectfully requested.

Since claim 14 is being cancelled, its dependent claims 15 – 18 are being amended to make them dependent upon claim 13. Claims 15 – 18 are therefore submitted to be allowable for the same reasons as claims 13.

Claims 19 – 23 and 25 – 33

Claims 19 – 25 stand rejected under 35 U.S.C. §103(a) over U.S. patents nos. 5,278,439 ("Ma et al.") and 6,137,718 ("Reisinger"). Two of these claims have been cancelled. Each of the remaining claims of this group has been amended. Reconsideration of the amended claims 19 – 23 and 25 is respectfully requested. Consideration of new claims 26 – 33, all being dependent upon this group of claims, is also respectfully requested.

The cited Ma et al. patent pertains to memory cells that store, on each of two conductive floating gates positioned over memory cell channels between their source and drain regions, one of two charge levels dependent upon the data being programmed. Each cell then stores two bits of data, one in each floating gate storage transistor. As the Office Action acknowledges, the Ma et al. patent does not disclose the use of a dielectric

material layer to store charge. The Reisinger patent, describing a memory cell with one dielectric charge storage element operated at more than two charge levels, is cited in the Office Action as evidence that this difference over the teachings of the Ma et al. patent would have been obvious.

But the claimed combination, it is respectfully submitted, would not have been rendered obvious from these two cited references. The dielectric of the Reisinger patent is programmed by Fowler-Nordheim tunneling. (Reisinger, col. 2, lns. 22-24, and col. 3, lns. 7-12 and 60-65). By this mechanism, electrons tunnel into the dielectric across the entire length of the channel region 4 of Reisinger since it is the electric field generated by the voltage difference between the substrate region 4 and gate electrode 6, both of which extend across the entire channel, that causes the tunneling. (See also section 1.2.1 of the Brown and Brewer book portion cited on page 2 of the present application, a copy of which has been made of record in this application.)

Each of claims 19 – 23 and 25 as amended, on the other hand, specify programming by either channel hot-electron injection or source side injection, two of the other programming mechanisms described in the cited Brown and Brewer book. These mechanisms cause electrons to be injected onto the floating gate to either its side nearest to the drain (channel hot-electron injection) or to its side nearest to the source (source side injection). Since the charge storage element of the Ma et al. memory cell is a conductive floating gate, charge injected onto a limited area of the floating gate is quickly redistributed across it. The resulting charge distribution is similar to that which results in Reisinger from Fowler-Nordheim programming into a dielectric storage element, where the charge does not migrate.

It is submitted, therefore, that it would not have been obvious to substitute dielectric charge storage elements for the floating gates of the Ma et al. reference in the manner claimed. To do so would have required operation of the Ma et al. system with Fowler-Nordheim programming in accordance with Reisinger, which is excluded by the claims as amended. The claims specify programming dielectric storage elements with charge in a localized region, as described in the present application (see Figures 9 and 12, for example). This is the result of either of the two programming mechanisms specified in the claims. Nothing has been noted in either of the Ma et al. or Reisinger references

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that suggests changing the programming technique of Reisinger to that of Ma et al. in order to obtain such localized charge storage regions. To the contrary, is seems that the Fowler-Nordheim charge storage system of Reisinger would have been maintained in any such combination in order to provide a charge distribution in the charge storing dielectric across the entire channel as exists with the conductive floating gates of the Ma et al. reference. The Reisinger reference clearly and strongly emphasizes Fowler-Nordheim tunneling rather than either of the alternative programming mechanisms claimed.

This is particularly true when specifying multi-state storage, i.e. more than one bit stored in each of the charge storage regions (claims 22, 25 and 33/25). Since Ma et al. does not discuss multi-state storage but Reisinger does, the mechanism for multi-state storage in a dielectric would be Reisinger's Fowler-Nordheim programming, which is outside the scope of these claims.

Others of the dependent claims add further features not suggested by the two cited references. For example, claim 20 recites that the dielectric is continuous across the length of the channel between source and drain regions. Replacement of the floating gates of Ma et al. with charge storage elements of Reisinger would not result in such a structure.

Dependent claims 27, 28 and 32 each recite that the control gate in the middle are recessed into the substrate. This is not suggested by either of the cited Ma et al. or Reisinger references.

Dependent claim 31 also adds further novelty by specifying that only two gates and dielectric storage elements exist in the individual cells, and that the two gates are attached to lines that extend perpendicularly to each other across the array. The embodiment of the present invention in Figures 7 – 9 describes this. Neither Ma et al. nor Reisinger suggest such an array of two storage element cells.

New Claims 34 – 36

Independent claim 34 is also directed to the embodiment of Figures 7 – 9. Orthogonally oriented conductive control and word lines form gates extending over the entire channel lengths of the memory cells. This is not suggested by any of the references cited in the Office Action to reject others of the claims.

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Information Disclosure Statement

The consideration of the references cited in the Information Disclosure Statement dated April 5, 2002, is noted with appreciation. Additionally, a Supplemental Information Disclosure Statement was filed by Express Mail on October 21, 2002, citing four additional references. Further, a Second Supplemental Information Disclosure Statement, with copies of references, is being filed herewith. Consideration of these additional references, and the making them of record in the file of this application, are respectfully requested.

Conclusion

It is believed, for the reasons given above, that each of the remaining claims 13, 15 – 23 and 25 - 36 is allowable. Therefore, an early indication of the allowance of the present application is solicited. However, if the Examiner has any further issues that need to be considered, he is invited to telephone the undersigned attorney at 415-217-6293 (direct dial).

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Respectfully submitted,

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AMENDED CLAIMS WITH MARKINGS TO SHOW CHANGES MADE

13.   (Amended)   A non-volatile memory of a type including an array of memory cells that individually has a charge storing dielectric material positioned between a conductive gate electrode and a surface of a substrate within a semi-conducting channel that extends across the surface between source and drain regions, comprising:

programming means including voltage sources connectable with the gates, sources and drains for transferring charge to at least ~~one~~ two defined regions of the charge storing dielectric of individual addressed ones of the memory cells by one of channel hot-electron injection or source-side injection to levels that adjust ~~a~~ thresholds of each of the at least ~~one~~ two defined portions of their individual channels to one of more than two threshold levels corresponding to the data being programmed, thereby to store more than one bit of such data in each of the at least two defined regions of the dielectric storage material of individual ones of the cells, and

reading means including voltage sources and sense amplifiers connectable with the gates, sources and drains of individual cells for ~~generating a parameter~~monitoring a level of current passing through the addressed cells between their source and drain regions in order to measure ~~that is related to~~ the programmed one of more than two threshold levels of each of the at least two defined regions of the individual cells.

15.   (Amended)   The memory of claim ~~14~~13, wherein the charge storage dielectric includes silicon nitride.

16.   (Amended)   The memory of claim ~~14~~13, wherein the charge storage dielectric includes silicon rich silicon dioxide.

17.   (Amended)   The memory of claim ~~14~~13, wherein said more than two defined ranges includes exactly four ranges of charge.

18.   (Amended)   The memory of claim ~~14~~13, wherein said more than two defined ranges includes more than four ranges of charge.

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19.   (Amended)   A non-volatile memory system, comprising:

an array of memory cells, wherein the individual memory cells include:

a channel having a length extending between source and drain regions within a substrate surface,

at least first and second conductive gates positioned over different portions of the channel along its length, and

at least first and second storage elements of dielectric charge trapping material sandwiched between respective ones of said at least first and second control gates and said substrate,

a programming circuit including a source of voltages connectable to the source and drain regions and to at least first and second gates that of addressed cells to causes electrons to be transferred from the substrate into said at least first and second storage elements by channel hot-electron injection or source-side injection to a storage level according to data being programmed, and

a reading circuit including a sense amplifiers connectable to at least one of the source and drain regions of addressed cells for determining a single the storage level of charge stored in each of said at least first and second storage elements including monitoring a level of current passing through the addressed cells between the source and drain regions.

20.   (Amended)   The memory system of claim 19, wherein said individual memory cells have their at least first and second storage elements are formed from a layer of the charge trapping material extending continuously across the length of the channel between the source and drain regions.

21.   (Amended)   The memory system of claim 19, wherein the individual memory cells additionally include a select transistor third control gate positioned between said at least first and second storage elements along the length of the channel and coupled with the channel through a gate a layer of dielectric sandwiched therebetween.

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22.   (Amended)   The memory system of any one of claims 19 - 21, wherein the programming circuit includes a source of voltages that causes electrons to be transferred into each of said at least first and second storage elements to one of more than two defined ~~ranges~~ storage levels according to more than one bit of data being stored, and wherein the reading circuit includes sense amplifiers connectable to at least the source or the drain for ~~identifying~~ determining the storage levels ~~of charge within~~ of one of more than two defined ranges stored in each of said at least first and second charge storage elements.

23.   (Amended)   A non-volatile memory, comprising:

elongated source and drain ~~diffusions~~ regions formed in a semiconductor substrate with their lengths extending in a first direction thereacross and being spaced apart in a second direction, the first and second directions being perpendicular to each other, thereby defining memory cell channels in the substrate between adjacent diffusions,

conductive control gates having lengths extending in the first direction, being positioned in the second direction over channel regions immediately adjacent the diffusions and being spaced apart in the second direction over an intermediate region of the cell channels,

dielectric charge storage material positioned at least between the control gates and a surface of the substrate within the memory cell channels, thereby to ~~form~~ provide at least two charge storage ~~transistors~~ regions in the dielectric charge storage material under the control gates in the memory cell channels ~~adjacent the diffusions, and~~

conductive word lines having lengths extending in the second direction and being spaced apart in the first direction, the word lines further being positioned over the control gates and extending therebetween over the intermediate channel regions ~~to provide gates for select transistors in the channels between the two storage transistors.~~,

a programming circuit including a source of programming voltages connectable to the source and drain regions, control gates and word lines for adding charge by channel hot-electron injection or source-side injection to the charge storage regions of the dielectric storage material to a storage level according to data being stored, and

a reading circuit including sense amplifiers connectable to at least the source and drain regions for determining the storage level of the individual charge storage regions by monitoring a level of current passing through the individual cells between the source and drain regions.

25.   (Amended)   The non-volatile memory of claim ~~24~~23, wherein the programming circuit operates to transfer charge into ~~said more than two defined ranges within a~~ common regions of the individual charge storage elements~~dielectric material~~ in more than two defined storage levels according to more than one bit of data being stored therein, and wherein the reading circuit operates to determine the storage levels of one of the more than two defined storage levels, thereby to read more than one bit of data from the individual common regions of the charge storage elements.

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